

1. An integrated circuit chip comprising:
  - semiconductor device structures in and on a substrate;
  - a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes contact pads;
  - a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;
  - a metal cap overlying each of said contact pads through an opening in said topmost passivation layer; and
  - a gold pad overlying said metal cap.
2. The integrated circuit according to Claim 1 further comprising a barrier layer overlying said metal cap and underlying said gold pad.
3. The integrated circuit according to Claim 1 wherein said metal cap comprises aluminum.
4. The integrated circuit according to Claim 2 wherein said barrier layer comprises titanium, titanium tungsten, titanium nitride, tantalum, tantalum nitride, or chromium.
5. The integrated circuit according to Claim 1 further comprising a wire bond formed on said gold pad.

6. The integrated circuit according to Claim 5 wherein said gold pad further extends from said underlying metal cap and wherein said wire bond is formed on a region of said extended gold pad.

7. The integrated circuit according to Claim 6 wherein said region for said wire bond is located over said semiconductor device structures.

8. The integrated circuit according to Claim 1 wherein said gold pad is used for testing.

9. The integrated circuit according to Claim 8 wherein said gold pad further extends from said underlying metal cap and wherein a region of said extended gold pad is used for testing.

10. The integrated circuit according to Claim 9 wherein said region for said testing is located over said semiconductor device structures.

11. A method of fabricating an integrated circuit chip comprising:

providing semiconductor device structures in and on a substrate;

providing a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device

structures wherein a topmost level of said interconnection lines includes contact pads;

providing a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

providing vias through said passivation layer to said contact pads;

providing a metal cap overlying each of said contact pads; and

forming post-passivation structures overlying said passivation layer and connected to said contact pads.

12. The integrated circuit according to Claim 11 wherein said metal cap comprises aluminum or an aluminum alloy.

13. The method according to Claim 11 wherein said post-passivation structures comprise wirebond pads, test pads, post-passivation interconnections, and/or passive components.

14. The method according to Claim 13 wherein said wirebond pads are formed by fabricating a gold pad overlying said metal cap and connecting a wire bond to said gold pad.

15. The method according to Claim 14 further comprising providing a barrier layer overlying said metal cap and underlying said gold pad.

16. The method according to Claim 15 wherein said barrier layer comprises titanium, titanium tungsten, titanium nitride, tantalum, tantalum nitride, or chromium.

17. The method according to Claim 14 wherein said wire bond comprises gold.

18. The method according to Claim 13 wherein said wirebond pads are formed by:

fabricating a gold pad which is laterally displaced from said metal cap;

further connecting said gold pad to said metal cap through a gold metal line; and

connecting a wire bond to said gold pad.

19. The method according to Claim 18 wherein said gold pad for said wire bond is located over said semiconductor device structures.

20. The method according to Claim 13 wherein said test pads are formed by fabricating a gold pad overlying said metal cap and making contact to said gold pad during testing.

21. The method according to Claim 20 further comprising providing a barrier layer overlying said metal cap and underlying said gold pad.

22. The method according to Claim 21 wherein said barrier layer comprises titanium, titanium tungsten, titanium nitride, tantalum, tantalum nitride, and chromium.

23. The method according to Claim 13 wherein said test pads are formed by:  
    fabricating a gold pad which is laterally displaced from said metal cap;  
    further connecting said gold pad to said metal cap through a gold metal line, and  
    making contact to said gold pad during testing.

24. The method according to Claim 23 wherein said gold pad for said wire bond is located over said semiconductor device structure.

25. A method of fabricating an integrated circuit chip comprising:  
    providing semiconductor device structures in and on a substrate;  
    providing a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes contact pads;  
    providing a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;  
    providing vias through said passivation layer to said contact pads;  
    providing a metal cap overlying each of said contact pads;

forming one or more metal lines in a first metal layer over said passivation layer, said one or more metal lines connected to said metal caps.

26. The method according to Claim 25 further comprising providing a barrier layer overlying said metal caps and underlying said first metal layer.

27. The method according to Claim 26 wherein said one or more metal lines comprise gold and said barrier layer comprises titanium tungsten.

28. The method according to Claim 26 wherein said one or more metal lines comprise copper and said barrier layer comprises chromium, titanium, titanium nitride, or titanium tungsten.

29. The method according to Claim 25 wherein said one or more metal lines comprise gold or copper.

30. The method according to Claim 29 wherein said one or more metal lines is formed by electroplating to a thickness greater than about 1  $\mu\text{m}$ .

31. A method of fabricating an integrated circuit chip comprising:

providing semiconductor device structures in and on a substrate;

providing a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device

structures wherein a topmost level of said interconnection lines includes contact pads;

providing a passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

providing vias through said passivation layer to said contact pads;

providing a metal cap overlying each of said contact pads;

forming an inductor over said passivation layer and connected to said metal caps.

32. A method of fabricating an integrated circuit chip comprising:

providing semiconductor device structures in and on a substrate;

providing a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes contact pads;

providing a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

providing vias through said passivation layer to said contact pads;

providing a metal cap overlying each of said contact pads;

forming a first metal layer over said passivation layer and said metal caps to form a bottom electrode of a capacitor;

forming a capacitor dielectric layer overlying said bottom electrode; and

forming a second metal layer overlying said capacitor dielectric layer to form a top electrode of said capacitor.

33. A method of fabricating an integrated circuit chip comprising:

providing semiconductor device structures in and on a substrate;

providing a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes contact pads;

providing a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

providing vias through said passivation layer to said contact pads;

providing a metal cap overlying each of said contact pads;

forming a first post-passivation dielectric layer overlying said passivation layer and said metal caps; and

forming one or more metal lines in a first metal layer overlying said first post-passivation dielectric layer, said one or more metal lines extending through openings through said first post-passivation dielectric layer to said metal caps.

34. The method according to Claim 33 further comprising forming a first barrier layer underlying said first metal layer.

35. The method according to Claim 34 wherein said first metal layer comprises gold and said first barrier layer comprises titanium tungsten.

36. The method according to Claim 34 wherein said first metal layer comprises copper and said first barrier layer comprises chromium, titanium, titanium nitride, or titanium tungsten.

37. The method according to Claim 33 wherein said first metal layer comprises gold or copper.

38. The method according to Claim 33 further comprising:

providing first metal contact pads in said first metal layer;

forming a second post-passivation dielectric layer overlying said first metal layer; and

forming openings in said second post-passivation dielectric layer to expose said first metal contact pads.

39. The method according to Claim 33 further comprising:

forming a second post-passivation dielectric layer overlying said first metal layer and forming one or more metal lines in a second metal layer overlying said second post-passivation dielectric layer, extending through openings through said second post-passivation dielectric layer to said first metal layer.

40. The method according to Claim 39 further comprising providing a second barrier layer underlying said second metal layer.

41. The method according to Claim 40 further comprising:

providing second metal contact pads in said second metal layer;

forming a third post-passivation dielectric layer overlying said second metal layer; and

forming openings in said third post-passivation dielectric layer to expose said second metal contact pads.

42. A method of fabricating an integrated circuit chip comprising:

providing semiconductor device structures in and on a substrate;

providing a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes contact pads;

providing a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

providing vias through said passivation layer to said contact pads;

providing a metal cap overlying each of said contact; and

forming a resistor overlying said passivation layer and connected to said metal caps.

43. The method according to Claim 42 further comprising a metal layer connecting said resistor to said metal caps

44. The method according to Claim 43 wherein said metal layer comprises gold or copper.

45. A method of fabricating an integrated circuit chip comprising:

- providing semiconductor device structures in and on a substrate;

- providing a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures wherein a topmost level of said interconnection lines includes contact pads;

- providing a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

- providing vias through said passivation layer to said contact pads;

- providing a metal cap overlying each of said contact pads;

- forming a barrier metal on said metal caps;

- forming solder pads on said barrier metal; and

- mounting discrete passive components on said solder pads.

46. The method according to Claim 45 further comprising:

- providing a post-passivation dielectric layer overlying said passivation layer and said metal caps;

forming openings in said post-passivation dielectric layer exposing said metal caps; and

forming said barrier metal within said openings in said post-passivation dielectric layer to said metal caps.

47. An integrated circuit chip comprising:

semiconductor device structures in and on a substrate;

a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting said semiconductor device structures;

a topmost passivation layer overlying said plurality of levels of interconnection lines and interlevel dielectric materials;

a metal cap overlying each of a topmost of said interconnection lines through an opening in said topmost passivation layer;

at least one first gold pad overlying a first subset of said metal caps wherein a wire bond overlies each of said first gold pads;

at least one second gold pad overlying a second subset of said metal caps wherein each of said second gold pads is used for testing said integrated circuit; and

a metal line overlying a third subset of said metal caps and connecting to contact pads underlying said third subset of metal caps.

48. The integrated circuit according to Claim 47 further comprising a barrier layer overlying said metal caps and underlying said gold pads and said metal line.

49. The integrated circuit according to Claim 47 wherein said metal cap comprises aluminum.

50. The integrated circuit according to Claim 48 wherein said barrier layer comprises titanium tungsten, titanium nitride, tantalum nitride, or chromium.

51. The integrated circuit according to Claim 47 further comprising:  
an inductor overlying said passivation layer and connecting to a fourth subset of said metal caps.

52. The integrated circuit according to Claim 47 further comprising:  
a resistor overlying said passivation layer and connecting to a fifth subset of said metal caps.

53. The integrated circuit according to Claim 47 further comprising:  
a capacitor overlying said passivation layer wherein a bottom and a top electrode of said capacitor connects to a sixth subset of said metal caps.

54. The integrated circuit according to Claim 47 further comprising:  
a discrete capacitor mounted on solder pads formed on a seventh subset of said metal caps.

55. The integrated circuit according to Claim 47 further comprising a post-passivation interconnection layer overlying said passivation layer and connecting to said metal caps.

56. A semiconductor device structure, comprising:

semiconductor devices formed on a semiconductor substrate, with an overlying interconnecting metallization structure connected to said devices and comprising a plurality of first metal lines, and having a passivation layer formed thereover, with first openings in said passivation layer to contact pads connected to said first metal lines, wherein said first openings are as small as 0.1  $\mu\text{m}$ ;

a metal cap on each of said contact pads within each of said first openings; and

a top metallization system formed over said passivation layer and said metal caps, connected to said metal caps and said interconnecting metallization structure, wherein said top metallization system comprises a plurality of top metal lines, in one or more layers, having a thickness substantially greater than said first metal lines.

57. The semiconductor device structure according to Claim 56 wherein said top metal lines comprise electroplated gold (Au) over a sputtered metal underlayer.

58. The semiconductor device structure according to Claim 56 wherein said top metal lines comprise electroplated copper (Cu) over a sputtered metal underlayer

59. The semiconductor device structure according to Claim 58 wherein said electroplated copper is covered with a nickel (Ni) cap layer.

60. The semiconductor device structure according to Claim 56 wherein said metal cap comprises aluminum.

61. A post passivation system, comprising:

a semiconductor substrate, having at least one interconnect metal layer over said semiconductor substrate, and a passivation layer over the at least one interconnect metal layer, wherein the passivation layer comprises at least one passivation opening through which is exposed at least one top level metal contact point;

a metal cap formed over said exposed at least one top level metal contact point; and

a passive component formed over said passivation layer and connected to said at least one top level metal contact point through said metal cap wherein said passivation opening's width is larger than about 0.1  $\mu\text{m}$ .

62. The post-passivation system according to Claim 61 wherein said metal cap comprises aluminum.

63. The post-passivation system according to Claim 61 further comprising metal interconnections, formed of a same material as said passive component and formed over said passivation layer, and connected to at least one of said top level metal contact points through said metal cap.

64. The post-passivation system according to Claim 61 wherein said passive component is a resistor, capacitor, or inductor.

65. A post passivation system, comprising:

- a semiconductor substrate, having at least one interconnect metal layer over said semiconductor substrate, and a passivation layer over the at least one interconnect metal layer, wherein the passivation layer comprises at least one passivation opening through which is exposed at least one top level metal contact point;

- a metal cap formed over said exposed at least one top level metal contact point; and

- a discrete component formed over said passivation layer and connected to said at least one top level metal contact point through said metal cap wherein said passivation opening's width is larger than about 0.1  $\mu\text{m}$ .

66. The post-passivation system according to Claim 65 wherein said metal cap comprises aluminum.

67. The post-passivation system according to Claim 65 further comprising metal interconnections formed over said passivation layer, and connected to at least one of said top level metal contact points through said metal cap.

68. The post-passivation system according to Claim 65 wherein said discrete component is a resistor, capacitor, or inductor.